REMARKS

The Office Action dated November 20, 2003, has been received and carefully considered. Claims 1-21 are pending in the present application. Reconsideration of the outstanding objections/rejections in the present application is respectfully requested based on the following remarks.

Applicants note with appreciation the indication on page 4 of the Office Action that claims 4, 5, 11, 13, and 19-21 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. However, Applicants have opted to defer rewriting the above-identified claims in independent form pending consideration of the arguments presented below with respect to the rejected claims.

I. THE ANTICIPATION REJECTION OF CLAIMS 1-3, 6-10, 12, & 14-18

On pages 2-4 of the Office Action, claims 1-3, 6-10, 12, and 14-18 were rejected under 35 U.S.C. § 102(b) as being anticipated by Gruetzner et al. (U.S. Patent No. 5,444,715). This rejection is hereby respectfully traversed.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished).

Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id.. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id..

Regarding claim 1, the Examiner asserts that Gruetzner et al. teach a transmit circuit, the transmit circuit comprising a transmit data input and a transmit data output, the transmit circuit producing a transmit data output signal at the transmit data output based on a transmit data input signal from the transmit data input when the transmit circuit is operating in a normal mode (the Examiner refers to column 4, lines 25-53; and Figure 1, items 111 and 127). However, item 111 in Figure 1 of Gruetzner et al. is specifically described as a receiving circuit, and item 127 in Figure 1 of Gruetzner et al. is

specifically described as an output of the receiving circuit. This is obviously in contrast to the present claim language, which is directed specifically to a transmit circuit.

As stated in MPEP § 2131, "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Also, as stated in MPEP § 2112, "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993). Accordingly, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, identify by reference number the exact component(s) in Gruetzner et al. that correspond to a transmit circuit comprising a transmit data input and a transmit data

output, wherein the transmit circuit produces a transmit data output signal at the transmit data output based on a transmit data input signal from the transmit data input when the transmit circuit is operating in a normal mode, as claimed.

The Examiner also asserts that Gruetzner et al. teach the transmit circuit further comprising a transmit repeating pattern generator producing a repeating pattern signal, the transmit circuit producing the transmit data output signal at the transmit data output based on the repeating pattern signal when the transmit circuit is operating in a test mode (the Examiner refers to columns 2-3, lines 49-38; column 4, lines 25-53; and Figure 2). However, it is respectfully submitted that Gruetzner et al. do not disclose or even suggest a transmit repeating pattern generator producing a repeating pattern signal as claimed. In fact, the closest Gruetzner et al. come to teaching a transmit repeating pattern generator for producing a repeating pattern signal, is a teaching that random test data may be scanned-in a scan-path of a sending chip and that an AC interconnect test may be repeated several times (see column 3, lines 30-32). This is clearly not a teaching of a transmit repeating pattern generator producing a repeating pattern signal as claimed. Thus, again, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a

prima facie case of anticipation, identify by reference number the exact component(s) in Gruetzner et al. that correspond to a transmit circuit further comprising a transmit repeating pattern generator producing a repeating pattern signal, wherein the transmit circuit produces the transmit data output signal at the transmit data output based on the repeating pattern signal when the transmit circuit is operating in a test mode, as claimed.

Similarly, the Examiner further asserts that Gruetzner et al. teach a receive circuit comprising a receive repeating pattern generator producing a repeating pattern signal, the receive circuit producing a comparison signal based on a comparison dependent on the transmit data output signal and the repeating pattern signal when the receive circuit is operating in the test mode (the Examiner refers to columns 2-3, lines 49-38; column 4, lines 25-53; and Figure 2). However, it is respectfully submitted that Gruetzner et al. do not disclose or even suggest a receive repeating pattern generator producing a repeating pattern signal as claimed. In fact, the closest Gruetzner et al. come to teaching a receive repeating pattern generator for producing a repeating pattern signal, is a teaching that random test data may be scanned-in a scan-path of a sending chip and that an AC interconnect test may be repeated several times (see column 3, lines 30-32). This is clearly not

a teaching of a receive repeating pattern generator producing a repeating pattern signal as claimed. Thus, again, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, identify by reference number the exact component(s) in Gruetzner et al. that correspond to a receive circuit comprising a receive repeating pattern generator producing a repeating pattern signal, wherein the receive circuit produces a comparison signal based on a comparison dependent on the transmit data output signal and the repeating pattern signal when the receive circuit is operating in the test mode, as claimed.

Accordingly, it is respectfully submitted that Gruetzner et al. does not anticipate the present invention as recited in claim 1.

Regarding claims 2, 3, and 6-8, these claims are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2, 3, and 6-8 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 2 recites that the transmit repeating pattern generator comprises a transmit shift register

and the receive repeating pattern generator comprises a receive shift register. The Examiner asserts that Gruetzner et al. teach that a repeating pattern generator may be implemented by a shift register (the Examiner refers to columns 2-3, lines 49-37). However, since Gruetzner et al. do not even teach a repeating pattern generator, as discussed above, Gruetzner et al. can not teach a repeating pattern generator being implemented by a shift register. Furthermore, the context in which Gruetzner et al. discuss shift registers is such that the shift registers are used for shifting arbitrary test data (see column 3, lines 4-6), not for producing a repeating pattern signal as claimed. Thus, again, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, identify by reference number the exact component(s) in Gruetzner et al. that correspond to a transmit repeating pattern generator comprising a transmit shift register and a receive repeating pattern generator comprising a receive shift register, as claimed.

Also, claim 3 recites that a transmit shift register output of the transmit shift register is coupled to a transmit shift register input of the transmit shift register when the transmit circuit is operating in the test mode, and that a receive shift register output of the receive shift register is coupled to a

receive shift register input of the receive shift register when the receive circuit is operating in the test mode. The Examiner asserts that Gruetzner et al. teach this limitation at columns 3-4, lines 49-37. However, since Gruetzner et al. do not even teach a repeating pattern generator, as discussed above, Gruetzner et al. can not teach a repeating pattern generator being implemented by a shift register. Furthermore, it is respectfully submitted that Gruetzner et al. do not claim, disclose, or even suggest the coupling arrangement (i.e., shift register outputs being coupled to shift register inputs when operating in test mode) as claimed. Thus, again, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, identify by reference number the exact component(s) in Gruetzner et al. that correspond to a transmit shift register output of a transmit shift register coupled to a transmit shift register input of the transmit shift register when the transmit circuit is operating in the test mode, and a receive shift register output of a receive shift register coupled to a receive shift register input of the receive shift register when the receive circuit is operating in the test mode, as claimed.

Furthermore, claim 6 recites that the transmit data output signal is capable of representing two bits of information

simultaneously over a single conductor. The Examiner asserts that item 124 in Figure 1 and Figure 2 of Gruetzner et al. teach this limitation. However, item 124 in Figure 1 of Gruetzner et al. is merely disclosed to be a line interconnecting sending chip 110 and receiving chip 111. Nowhere do Gruetzner et al. claim, disclose, or even suggest that a transmit data output signal is capable of representing two bits of information simultaneously over a single conductor. In fact, it is respectfully submitted that Gruetzner et al. cannot even support such a feature, which requires multi-level signaling capability. Thus, again, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, identify by reference number the exact component(s) in Gruetzner et al. that allow the transmit data output signal to represent two bits of information simultaneously over a single conductor, as claimed.

Furthermore, claim 8 recites that the transmit data output signal is communicated as a differential signal over two conductors. The Examiner asserts that items 120 and 121 in Figure 1 of Gruetzner et al. teach this limitation. However, items 120 and 121 in Figure 1 of Gruetzner et al. are merely disclosed to be lines interconnecting two separate master/slave devices 114 and 115 to a driver 122. Nowhere do Gruetzner et

al. claim, disclose, or even suggest that a transmit data output signal is communicated as a differential signal over two conductors. In fact, it is respectfully submitted that Gruetzner et al. cannot even support such a feature, which requires differential transmitters and receivers. Thus, again, Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, identify by reference number the exact component(s) in Gruetzner et al. that allow the transmit data output signal to be communicated as a differential signal over two conductors, as claimed.

Accordingly, it is respectfully submitted that Gruetzner et al. do not anticipate the present invention as recited in claims 2, 3, and 6-8.

Regarding claim 9, the Examiner asserts that Gruetzner et al. teach generating a transmit repeating pattern in a transmit circuit, and transmitting the transmit repeating pattern to a receive circuit (the Examiner refers to column 1 , lines 35-57; columns 2-3, lines 49-38). However, it is respectfully submitted that Gruetzner et al. do not disclose or even suggest generating a transmit repeating pattern in a transmit circuit, and transmitting the transmit repeating pattern to a receive circuit as claimed. In fact, the closest Gruetzner et al. come

to teaching generating a transmit repeating pattern in a transmit circuit, is a teaching that random test data may be scanned-in a scan-path of a sending chip and that an AC interconnect test may be repeated several times (see column 3, lines 30-32). This is clearly not a teaching of generating a transmit repeating pattern in a transmit circuit as claimed. Furthermore, the Examiner refers to column 1 , lines 35-57, of Gruetzner et al. to support his assertion, but this teaching (see column 1, lines 54-57) is specifically limited to testing individual chips (i.e., not interconnections between chips (e.g., systems)), which is totally in contrast to the present invention as claimed. Thus, Gruetzner et al. actually teach away from the present invention as claimed, since, as stated in MPEP § 2141.02, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

The Examiner also asserts that Gruetzner et al. teach generating a receive repeating pattern in the receive circuit, and comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison (the Examiner refers to column 1, lines 35-57; columns 2-3, lines 49-38). However, it

is respectfully submitted that Gruetzner et al. do not disclose or even suggest generating a receive repeating pattern in the receive circuit, and comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison as claimed. In fact, the closest Gruetzner et al. come to teaching generating a receive repeating pattern in the receive circuit, is a teaching that random test data may be scanned-in a scan-path of a sending chip and that an AC interconnect test may be repeated several times (see column 3, lines 30-32). This is clearly not a teaching of generating a receive repeating pattern in the receive circuit as claimed. Furthermore, the Examiner refers to column 1 , lines 35-57, of Gruetzner et al. to support his assertion, but this teaching (see column 1, lines 54-57) is specifically limited to testing individual chips (i.e., not interconnections between chips (e.g., systems)), which is totally in contrast to the present invention as claimed. Thus, Gruetzner et al. actually teach away from the present invention as claimed, since, as stated in MPEP § 2141.02, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

Accordingly, it is respectfully submitted that Gruetzner et al. does not anticipate the present invention as recited in claim 9.

Regarding claims 10, 12, and 14-18, these claims are dependent upon independent claim 9. Thus, since independent claim 9 should be allowable as discussed above, claims 10, 12, and 14-18 should also be allowable at least by virtue of their dependency on independent claim 9. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination. For example, claim 10 recites adjusting a parameter affecting operation of the transmit circuit based on the comparison. The Examiner asserts that Gruetzner et al. teach adjusting the characteristic of the circuit (the Examiner refers to column 1, lines 35-57; columns 2-3, lines 20-37; the abstract; and items 110 and 111 in Figure). However, Applicants could find no such teaching at column 1, lines 35-57, or anywhere else, of Gruetzner et al.. Thus, it is respectfully submitted that Gruetzner et al. fail to teach adjusting the characteristic of a circuit. More particularly, it is respectfully submitted that Gruetzner et al. fail to teach adjusting a parameter affecting operation of the transmit circuit based on the comparison as claimed. Thus, again,

Applicants respectfully request that the Examiner, in accordance with his duty to present at least a prima facie case of anticipation, identify by reference number the exact component(s) in Gruetzner et al. that allow for adjusting a parameter affecting operation of the transmit circuit based on a comparison, as claimed.

Also, claim 12 recites utilizing a shift register to generate the transmit repeating pattern, claim 14 recites transmitting the transmit repeating pattern as a signal referenced to a ground, claim 15 recites transmitting the transmit repeating pattern as a differential signal over a pair of conductors, claim 16 recites transmitting the transmit repeating pattern by encoding two bits of information on a single conductor simultaneously, claim 17 recites adjusting a receiver characteristic of the receive circuit, and claim 18 recites that the receiver characteristic is selected from a group consisting of a receiver circuit timing signal and a voltage reference. The Examiner does not address how any of these claim limitations are anticipated by Gruetzner et al.. Thus, it is respectfully submitted that the Examiner has failed to carry his burden of establishing even a prima facie case that each and every element of claims 12 and 14-18 is disclosed by the Gruetzner et al..

Accordingly, it is respectfully submitted that Gruetzner et al. does not anticipate the present invention as recited in claims 10, 12, and 14-18.

At this point, the Applicants would like to address the assertion made by the Examiner that "during patent examination, the pending claims must be given the broadest reasonable interpretation consistent with the specification." Applicants agree with this assertion. Indeed, when the present pending claims are given the broadest reasonable interpretation consistent with the specification, it is still clear that Gruetzner et al. do not teach the claimed limitations. In the simplest terms, Gruetzner et al. do not claim, disclose or even suggest a transmit circuit operably coupled to a receive circuit, wherein the transmit circuit comprises a transmit data input and a transmit data output, wherein the transmit circuit produces a transmit data output signal at the transmit data output based on a transmit data input signal from the transmit data input when the transmit circuit is operating in a normal mode, wherein the transmit circuit further comprises a transmit repeating pattern generator producing a repeating pattern signal, wherein the transmit circuit produces the transmit data output signal at the transmit data output based on the repeating pattern signal when the transmit circuit is operating in a test

mode, wherein the receive circuit receives the transmit data output signal from the transmit circuit at a receive data input, wherein the receive circuit comprises a receive data output, wherein the receive circuit produces a receive data output signal at the receive data output based on the transmit data output signal when the receive circuit is operating in the normal mode, wherein the receive circuit further comprises a receive repeating pattern generator producing the repeating pattern signal, and wherein the receive circuit produces a comparison signal based on a comparison dependent on the transmit data output signal and the repeating pattern signal when the receive circuit is operating in the test mode. Similarly, Gruetzner et al. do not claim, disclose or even suggest generating a transmit repeating pattern in a transmit circuit, transmitting the transmit repeating pattern to a receive circuit, generating a receive repeating pattern in the receive circuit, and comparing the transmit repeating pattern to the receive repeating pattern to obtain a comparison. Thus, there is no need to amend the present pending claims.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1-3, 6-10, 12, and 14-18 be withdrawn.

II. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

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APPENDIX A

1 (Previously Presented). A digital signaling system comprising:

a transmit circuit, the transmit circuit comprising a transmit data input and a transmit data output, the transmit circuit producing a transmit data output signal at the transmit data output based on a transmit data input signal from the transmit data input when the transmit circuit is operating in a normal mode, the transmit circuit further comprising a transmit repeating pattern generator producing a repeating pattern signal, the transmit circuit producing the transmit data output signal at the transmit data output based on the repeating pattern signal when the transmit circuit is operating in a test mode; and

a receive circuit, the receive circuit operably coupled to the transmit circuit and receiving the transmit data output signal from the transmit circuit at a receive data input, the receive circuit comprising a receive data output, the receive circuit producing a receive data output signal at the receive data output based on the transmit data output signal when the receive circuit is operating in the normal mode, the receive circuit further comprising a receive repeating pattern generator producing the repeating pattern signal, the receive circuit

producing a comparison signal based on a comparison dependent on the transmit data output signal and the repeating pattern signal when the receive circuit is operating in the test mode.

2 (Original). The digital signaling system of claim 1 wherein the transmit repeating pattern generator comprises a transmit shift register and the receive repeating pattern generator comprises a receive shift register.

3 (Previously Presented). The digital signaling system of claim 2 wherein a transmit shift register output of the transmit shift register is coupled to a transmit shift register input of the transmit shift register when the transmit circuit is operating in the test mode and a receive shift register output of the receive shift register is coupled to a receive shift register input of the receive shift register when the receive circuit is operating in the test mode.

4 (Previously Presented). The digital signaling system of claim 2 wherein the transmit circuit further comprises a transmit linear feedback logic gate, wherein a first transmit shift register output of the transmit shift register is coupled to a first transmit linear feedback logic input of the transmit

linear feedback logic gate, and wherein a second transmit shift register output of the transmit shift register is coupled to a second transmit linear feedback logic input of the transmit linear feedback logic gate, the transmit linear feedback logic gate producing a transmit linear feedback logic gate output signal upon which a transmit shift register input signal at a transmit shift register input of the transmit shift register depends when the transmit circuit is operating in the test mode, and wherein the receive circuit further comprises a receive linear feedback logic gate, wherein a first receive shift register output of the receive shift register is coupled to a first receive linear feedback logic input of the receive linear feedback logic gate, and wherein a second receive linear feedback logic input of the receive linear feedback logic gate, the receive linear feedback logic gate producing a receive linear feedback logic gate output signal upon which a receive shift register input signal at a receive shift register input of the receive shift register depends when the receive circuit is operating in the test mode.

5 (Original). The digital signaling system of claim 1 wherein the transmit repeating pattern generator comprises a transmit linear feedback shift register and the receive repeating pattern

generator comprises a receive linear feedback shift register.

6 (Original). The digital signaling system of claim 1 wherein the transmit data output signal is capable of representing two bits of information simultaneously over a single conductor.

7 (Original). The digital signaling system of claim 1 wherein the transmit data output signal is communicated over a single conductor referenced to a ground voltage.

8 (Original). The digital signaling system of claim 1 wherein the transmit data output signal is communicated as a differential signal over two conductors.

9 (Original). A method for evaluating a digital signaling system comprising the steps of:

generating a transmit repeating pattern in a transmit circuit;

transmitting the transmit repeating pattern to a receive circuit;

generating a receive repeating pattern in the receive circuit; and

comparing the transmit repeating pattern to the receive

repeating pattern to obtain a comparison.

10 (Original). The method of claim 9 further comprising the steps of:

adjusting a parameter affecting operation of the transmit circuit based on the comparison.

11 (Original). The method of claim 10 wherein the parameter is selected from a group consisting of an output current, a crosstalk cancellation coefficient, and a self-equalization coefficient.

12 (Original). The method of claim 9 wherein the step of generating a transmit repeating pattern in a transmit circuit comprises the step of:

utilizing a shift register to generate the transmit repeating pattern.

13 (Original). The method of claim 12 wherein the step of utilizing a shift register to generate the transmit repeating pattern comprises the step of:

utilizing a linear feedback shift register to generate the transmit repeating pattern.

14 (Original). The method of claim 9 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

transmitting the transmit repeating pattern as a signal referenced to a ground.

15 (Original). The method of claim 9 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

transmitting the transmit repeating pattern as a differential signal over a pair of conductors.

16 (Original). The method of claim 9 wherein the step of transmitting the transmit repeating pattern to the receive circuit further comprises the step of:

transmitting the transmit repeating pattern by encoding two bits of information on a single conductor simultaneously.

17 (Original). The method of claim 9 further comprising the step of:

adjusting a receiver characteristic of the receive circuit.

18 (Previously Presented). The method of claim 17 wherein the receiver characteristic is selected from a group consisting of a receiver circuit timing signal and a voltage reference.

19 (Original). The method of claim 17 further comprising the step of:

determining boundary values of the receiver characteristic within which reliable operation of the system is provided.

20 (Previously Presented). The method of claim 19 further comprising the step of:

adjusting a parameter affecting operation of the transmit circuit based on the boundary values.

21 (Original). The method of claim 20 wherein the parameter is selected from a group consisting of an output current, a crosstalk cancellation coefficient, and a self-equalization coefficient.